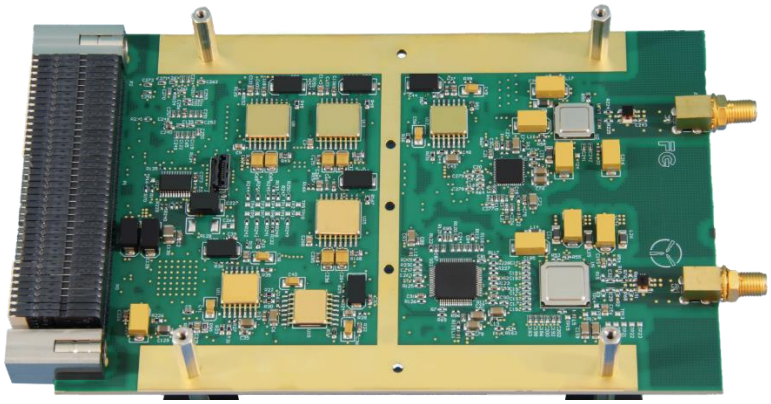

Introduction

The Frontgrade™ SRFM-PS is a 600-2600MHz RF bandwidth module providing reliable direct-to-digital conversion of L/S-band RF signals. Leveraging Analog Devices' AD9213S (ADC) and AD9176S (DAC), the SRFM-PS supports JESD204B Subclass 0 communication to the backplane of a system implementation. The compact 3U SpaceVPX based design is compatible with Frontgrade's 9-slot Reconfigurable Processing System (RPS-9x-PS) allowing systems add multiple channels and implement full software defined radios.

To collect and report telemetry as well as oversee the major components of the design and allow for implementation of additional radiation mitigation and error handling strategies, the SRFM-PS includes a Radiation Hardened ARM Cortex M0+ based Microcontroller with its own independent boot and application Flash Memory. The microcontroller also supports register settings of all major ICs on board to control clock generation and ADC/DAC settings.

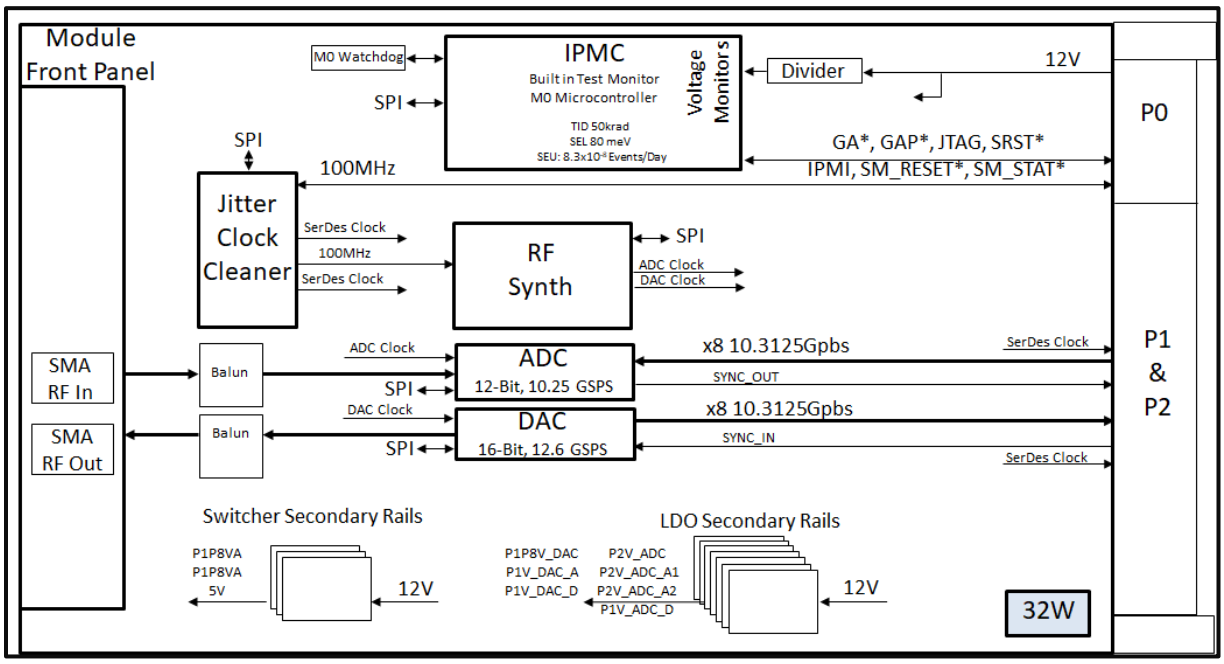

Figure 1. SRFM-PS Block Diagram

System RF Module: SRFM-PS

Features

AD9176S Digital to Analog Converter (DAC)

- 12.6 GSPS, 16-Bit Resolution, with interpolation
- 6.16 GSPS, 16-Bit Resolution, no interpolation
- Supports Real and Complex Data
- 48-bit NCO
- JESD204B x8
- 2-tone intermodulation distortion (IMD) = −83 dBc at 1.8 GHz, −7 dBFS/tone RF output
- Spurious free dynamic range (SFDR) <−80 dBc at 1.8 GHz, −7 dBFS RF output

AD9213S Analog to Digital Converter (ADC)

- 10.25 GSPS, 12-Bit Resolution, 6.5GHz bandwidth
- Integrated Digital Downconverter
- Supports Real and Complex Data
- 48-bit NCO
- JESD204B x8

Front Panel Interfaces

The SRFM Front Panel offers access to RF input and RF output through SMA connections.

- 1x RF Input (SMA)
- 1x RF Output (SMA)

Mass / Volume / Thermal

- Mass: <0.65kg, standard 3U SpaceVPX form factor
- -25°C to +65°C operational
- Power consumption: 31.5W as simulated

Backplane Panel Interfaces

- 8x ADC and DAC SERDES Lanes (JESD204B)
- 1x UART for microcontroller reprogramming
- 1x 100MHz reference clock input
- 1x IPMB interface with subset of IPMB commands supported
- 1x reset interface
- JESD204B signals
  - 1X DAC_SYNCOUT+/-,
  - 1X FPGA_SYSREF+/-,
  - 1X FPGA_REF_CLK+/-,
  - 1X ADC_TRIG+/-,
  - 1X ADC_SYNCIN+/-,
  - 1X ADC_SYNCIN_SE
- SpaceVPX peripheral slot profile (Slot Profile: SLT3-PAY-2T1Q-14.3.1)
- 12V Power Input

Operational Life / Reliability and Performance

- System reliability over 0.9
- System SEU rate: No more than one per year for typical LEO Missions
- TID of 25 krads (Si) or 100 krads (Si) optional assuming 100 mils of shielding with 6061-T6 Aluminum
- NASA PEM-INST-001 Level-2 parts pedigree available

Software

The SRFM is delivered with a default configuration of microcontroller code. This code will boot the device into a known state. The microcontroller code can be modified based on mission specific applications and data rates.