AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

PROBLEM ADVISORY

CAES

1. TITLE	2. DOCUMENT NUMBER
SMD 5962-17212 UPDATE; PIN C4 DESCRIPTION CHANGE; SER AND SEP CHANGE; I2C AND ADC SPECIFICATION AND VALUE UPDATES; PIN M2 TYPO CORRECTION	SPO-2020-PA-0007
	3. DATE *(Year, Month, Date)* 2020, SEPTEMBER, 17
4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	5. MANUFACTURER POINT OF CONTACT NAME Owen Watry
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8. CAGE CODE	9. LDC START	10. LDC END	11. PRODUCT IDENTIFICATION CODE	12. BASE PART
65342	ALL	ALL	QS30	TABLE 1

13. BLANK	14. SMD NUMBER	15. DEVICE TYPE DESIGNATOR
	17212	01, 02
	16. RHA LEVELS L	17. QML LEVEL Q
	18. NON QML LEVEL Proto, Hi-Rel, Lean-Rel, Q+	19. GIDEP NUMBER GB4-P-20-07

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

CAES is issuing this Problem Advisory (PA) to inform its customers about the changes made to the 5962-17212 Standard Microcircuit Drawing. See attached **TABLE 1** for the affected part numbers.

The following changes have been made to the SMD 5962-17212. The changes have been organized by their impact to the customer:

- Changes that could affect the reliability of the part and radiation tolerance of the NOR Flash if not addressed
  - Changes to the description/name of pin C4
- Changes to the form/fit/function of the device
  - Update to the SER Specification and relevant notes, and the SEP Test Limits Table 1B
  - Removal of I2C Hysteresis of Schmitt Trigger Inputs and ADC Input Leakage Current Specifications
  - Removal of the typical limits for ADC Integral Nonlinearity, Differential Nonlinearity, Offset Error, and Gain Error Specifications
  - Improvement to the ADC Gain Error Specification Minimum limit
  - Correction to the description/name of pin M2

Summaries of each change are detailed on the attached sheets.

21. ACTION TAKEN / PLANNED

CAES has already updated the UT32M0R500 datasheet located on its website (https://scss.cobhamaes.com/pagesproduct/prods-hirel-arm.cfm).

22. DISPOSITIONARY RECOMMENDATION:	CHECK & USE AS IS ☐	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CORRECT & USE AS SPECIFIED ☒

Table 1: Affected Part Numbers:

UT32M0R500-ZPC
UT32M0R500-ZFC
UT32M0R500LZLC
UT32M0R500-SPF
UT32M0R500-SFF
UT32M0R500LSLF
UT32M0R500LCLF
UT32M0R500-CPA
5962L1721201QXC
5962L1721201QYF
5962L1721202QXC
5962L1721202QYF

Changes to the description/name of pin C4:
Pin C4, previously labeled 'VDDN' is now labeled 'RESERVED'. Pin C4 was used as a test pin during development and characterization of the UT32M0R500. The pin monitors voltage internally generated by the microcontroller die to power the NOR Flash die. Per SMD and Datasheet documentation, the NOR Flash needs to be powered down for 90% of the mission life to ensure it meets the radiation requirements. Connecting pin C4 to a positive or ground voltage supply will prevent proper operation of the NOR Flash power supply, over-riding the internal power switching, potentially causing increased current within the part. As previously mentioned, tying C4 to a positive voltage supply will permanently power the NOR Flash, which impacts the TID tolerance of the device. Pin C4 must be left floating (No Connect) to ensure the proper operation of the part. If the part has been powered on with pin C4 tied to VDD for 10 or more hours at 85°C or above, contact the factory for the reliability impact.

Update to the SER Specifications and relevant notes:
The Heavy Ion Soft Error Rate (SER) specification has been changed from 2.8×10^{-12} error/bit-day to 8.3×10^{-8} error/device-day. This change is being made to correct for a calculation error made in the Adams 90% worst-case environment calculation. The original calculations for the SRAM Cross Section (cm^2/bit) due to a data entry issue had an extra "0" making them an order of magnitude off. This only pertains to SRAM numbers, the other per bit or per flop cross sections were not affected. In addition to the order of magnitude correction, the SRAM error rate calculation in the report had an additional error caused by an extra division by the number of bits. This error only affected the SRAM.

The SER reported in the datasheet and SMD refers to the intrinsic SEU rate of the SRAM, which was one of the error rates affected by the errors in the radiation report. The corrected intrinsic SEU rate is 4.65×10^{-6} errors/bit-day and not the 2.8×10^{-12} errors/bit-day reported. Because the microcontroller employs ECC and the user cannot bypass the ECC and access the SRAM directly, the value reported as SER in the SMD is not relevant to user applications. Therefore, the SER listed is being replaced with the soft reset event rate of the microcontroller, which is the most relevant error rate for the user. Appendix A lists error rates from the JEDEC standard JESD 79. The soft-reset event rate is equivalent to what JESD 79 lists as Soft Error, Device.

Removal of I2C Hysteresis of Schmitt Trigger Inputs and ADC Input Leakage Specification
The I2C Hysteresis of Schmitt Trigger Inputs specification has been removed because the UT32M0R500's I2C inputs are not actually Schmitt Triggers. The inclusion of this specification in the Datasheet and SMD was due to an oversight made during the design of this part to ensure our part was in compliance with the I2C specification.

The ADC Input Leakage Specification is being removed. The ADC inputs meet the IIHA and IIL/IIH specifications found in the I/O DC Specifications section, so this specification was redundant.

Removal of the typical limits for ADC Integral Nonlinearity, Differential Nonlinearity, Offset Error, and Gain Error Specifications
The Typical values listed have been removed from both the Datasheet and SMD. Additionally the notes "Typ @ PGA Gain = 1" have been corrected to say "PGA Gain = 1" for the Offset error and Gain Error specifications.

Improvement to the ADC Gain Error Specification Minimum limit
The ADC Gain Error Specification Minimum limit has been increased from -15% to -4%.

Correction to the description/name of pin M2
Pin M2 had a typo, and has been changed from MISO/GPIO44 to MISO/GPIO42.

Appendix A - Terms and definitions from JESD89

Single-event effect (SEE): Any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic-particle strike.
NOTE Single-event effects include single-event upset (SEU), multiple-bit SEU (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE), single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR).

Single-event functional interrupt (SEFI): A soft error that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not require power cycling of the device (off and back on) to restore operability, unlike single-event latch-up (SEL), or result in permanent damage as in single-event burnout (SEB).
NOTE An SEFI is often associated with an upset in a control bit or register.

Single-event gate rupture (SEGR): An event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET.
NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

Single-event hard error (SHE): An irreversible change in operation resulting from a single radiation event and typically associated with permanent damage to one or more elements of a device (e.g., gate oxide rupture).

Single-event latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle through sensitive regions of the device structure and resulting in the loss of device functionality.
NOTE 1 SEL may cause permanent damage to the device. If the device is not permanently damaged, power cycling of the device (off and back on) is necessary to restore normal operation.
NOTE 2 An example of SEL in a CMOS device occurs when the passage of a single particle induces the creation of parasitic bipolar (p-n-p-n) shorting of power to ground.

Single-event transient (SET): A momentary voltage excursion (voltage spike) at a node in an integrated circuit caused by the passage of a single energetic particle.

Single-event upset (SEU): A soft error caused by the transient signal induced by the passage of a single energetic particle.

Soft error, device: An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device containing the latch or memory cell.
NOTE 1 As commonly used, the term refers to an error caused by radiation or electromagnetic pulses and not to an error associated with a physical defect introduced during the manufacturing process.
NOTE 2 Soft errors can be generated from SEU, SEFI, MBU, MCU, and/or SET. The term SER, which includes a variety of soft error mechanisms, has been adopted by the commercial industry while the more specific terms SEU, SEFI, etc. are typically used by the avionics, space, and military electronics communities.

Soft error, power cycle (PCSE): A soft error that is not corrected by repeated reading or writing but can be corrected by the removal of power (e.g., nondestructive latch-up).

Soft error, static: A soft error that is not corrected by repeated reading but can be corrected by rewriting without the removal of power.

Soft error, transient: A soft error that can be corrected by repeated reading without rewriting and without the removal of power.