

# PRODUCT INFORMATION NOTICE

1. TITLE	2. DOCUMENT NUMBER	
UT54ACS162245SLV (MULTI-PURPOSE 3-VOLT TRANSCEIVER WITH COLD/WARM SPARE I/O)	SPO-2014-PIN-0004	
ADD POWER SEQUENCE OF VDD1/VDD2	3. DATE (Year, Month, Date) 2014, September, 5	
4. MANUFACTURER NAME AND ADDRESS CAES	5. MANUFACTURER POINT OF CONTACT NAME Fred Sievert	
4350 CENTENNIAL BOULEVARD	6. MANUFACTURER POINT OF CONTACT TELEPHONE	
COLORADO SPRINGS, COLORADO 80907-3486	(719) 594-8000	
	7. MANUFACTURER POINT OF CONTACT EMAIL	
	Sievert@cobhamaes.com	
8. CAGE CODE 9. BLANK 65342	10. PRODUCT IDENTIFICATION CODE WA04 & WA05	11. BASE PART UT54ACS162245SLV
12. BLANK	13. SMD NUMBER 5962-02543	14. DEVICE TYPE DESIGNATOR ALL
	15. RHA LEVELS	16. QML LEVEL
	ALL	ALL
	17. NON QML LEVEL	18. BLANK
	ALL	

<sup>19.</sup> DESCRIPTION (FOR NEW PRODUCTS, PROVIDE AVAILABILITY DATE AND LEAD TIME)

When powering VDD1 on the UT54ACS162245SLV ahead of VDD2, an increased quiescent current up to 150mA on the VDD1 supply occurs. The increased VDD1 supply current remains until VDD2 reaches 1.5V + -5%.

Add power application guidelines and power-up sequencing explanation to the datasheet and SMD.

# **Power Application Guidelines**

For proper operation connect power to all VDD pins and ground all VSS pins (i.e., no floating VDD or VSS supply pins). If VDD1 and VDD2 are not powered up together, then VDD2 should be powered up first to ensure proper control of /OEx and DIRx. Control of the outputs /OEx and DIRx pins is not guaranteed until VDD2 reaches 1.5 +/-5%. During normal operation of the device, after power up, insure VDD1≥VDD2.

### Power Up Sequence

Because the direction control (DIRx) and output enable (/OEx) pins on the UT54ACS162245SLV are powered by VDD2, user's should power-up VDD2 before VDD1. If VDD1 is powered on first, VDD2 must be powered on within 1 second of VDD1 reaching 1.5V +/-5%. An elevated VDD1 supply current up to 150mA will occur when VDD1 > 1.5V+/5% and VDD2 < 1.5V +/-5%.

# Warm Spare

Once the UT54ACS162245SLV is powered up with VDD1  $\geq$  VDD2, the application may place the device into "Warm Spare" mode by driving EITHER supply to VSS +/- 0.25V with a maximum 1K $\Omega$  impedance between VDDx and VSS. While in Warm Spare, the device places all outputs into a high impedance state (see DC electrical parameters, Iws).

#### **Cold Spare**

The  $U\bar{T}54ACS162245SLV$  places the device into "Cold Spare" mode when BOTH supplies are set to VSS +/- 0.25V with a maximum  $1K\Omega$  impedance between VDDx and VSS. While in Cold Spare, the device places all outputs into a high impedance state (see DC electrical parameters, Ics).

NOTE: THIS DOCUMENT IS PUBLISHED FOR INFORMATION PURPOSES AND MAY PROVIDE FORWARD LOOKING STATEMENTS THAT ARE SUBJECT TO CHANGE. THE USERS SHOULD CONTACT THEIR LOCAL CAES SALES OFFICE FOR ANY ACTIONABLE CONTENT DESCRIBED HEREIN.

20. ADEPT REPRESENTATIVE	21. SIGNATURE	22. DATE
Timothy L. Meade	Timothy Meade	September 12, 2014

ADEPT PIN FORM REVISON DATE: 05/28/2014 REVISION: B

Affected Part Numbers	
UT54ACS162245SLV-UPC	
UT54ACS162245SLV-UCC	
UT54ACS162245SLV-UCA	
5962R0254301QXC	
5962F0254301QXC	
5962R0254301QXA	
5962F0254301QXA	
5962R0254301VXC	
5962F0254301VXC	
5962R0254301VXA	
5962F0254301VXA	
5962H0254301QXC	
5962G0254301QXC	
5962H0254301QXA	
5962G0254301QXA	
5962H0254301VXC	
5962G0254301VXC	
5962H0254301VXA	
5962G0254301VXA	