AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

PROBLEM ADVISORY

CAES

1. TITLE	2. DOCUMENT NUMBER
MICROCIRUIT, MEMORY, DIGITAL, CMOS, 512K X 32-BIT (16M) WITH EMBEDDED EDAC, RADIATION-HARDENED LOW VOLTAGE SRAM, MONOLITHIC SILICON	SPO-2012-PA-0001
	3. DATE *(Year, Month, Date)*: 2012, October, 04
4. MANUFACTURER NAME AND ADDRESS: CAES, 4350 CENTENNIAL BOULEVARD, COLORADO SPRINGS, COLORADO 80907-3486	5. MANUFACTURER POINT OF CONTACT NAME: Mike Leslie
	6. MANUFACTURER POINT OF CONTACT TELEPHONE: (719) 594-8148
	7. MANUFACTURER POINT OF CONTACT EMAIL: Mike.Leslie@cobhamaes.com

8. CAGE CODE	9. LDC START	10. LDC END	11. PRODUCT IDENTIFICATION CODE	12. BASE PART
65342	ALL	ALL	WC04 / WC05	UT8ER512K32M/S
13. BLANK			14. SMD NUMBER: 5962-06261	15. DEVICE TYPE DESIGNATOR: TYPE (01-06)
			16. RHA LEVELS: R	17. QML LEVEL: Q, V
			18. NON QML LEVEL: HiRel, Protos	19. BLANK

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

The EDAC control register electrical performance characteristic parameter t_{AVCL} (Table 1A, sheet 10 of SMD: 5962-06261) min of 200ns is insufficient for reliable accesses to the EDAC control register settings. An incorrect test method resulted in inaccurate initial characterization data.

21. ACTION TAKEN / PLANNED

CAES' test methodology has been corrected. Device Characterization has been performed to verify compliance with the increased 400ns minimum specification. Additionally, parameters t_{CHAV} and t_{CLAX} specifications of 0ns minimum were added to clarify the EDAC control register sequence.

CAES is working in coordination with DLA Land and Maritime to effect the changes referenced in this ADEPT to the SMD, which is currently at revision level B.

The proposed list of SMD changes related to parameters t_{CHAV}, t_{CLAX}, and t_{AVCL} are appended to this GIDEP.

Fielded units are guaranteed by design to meet these parameters, no field returns are planned.

22. DISPOSITIONARY RECOMMENDATION:	USE AS IS ☐	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CHECK & USE AS IS ☒

23. ADEPT REPRESENTATIVE	24. SIGNATURE	25. DATE
Timothy L. Meade		**04, October, 2012**

TABLE IA. Electrical performance characteristics (sheet 10)

Previous:

Test	Symbol	Test condition	Group A subgroups	Device Type	Limits		Units
					min	max	
Address valid to control low	t_{AVCL}		9,10,11	All	200		ns

Corrected:

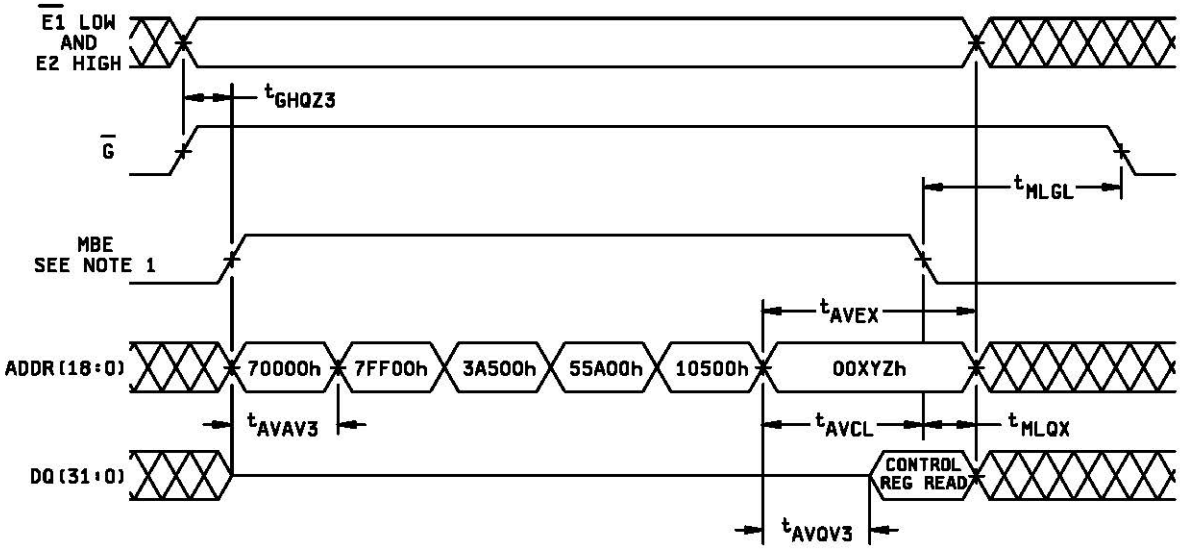
Test	Symbol	Test condition	Group A subgroups	Device Type	Limits		Units
					min	max	
Address valid to control low	t_{AVCL}		9,10,11	All	400		ns

Added parameter to TABLE IA. Electrical performance characteristics (sheet 10)

Test	Symbol	Test condition	Group A subgroups	Device Type	Limits		Units
					min	max	
MBE high to address valid	t_{CHAV}		9,10,11	All	0		ns
MBE low to address invalid	t_{CLAX}		9,10,11	All	0		ns

FIGURE 5. Timing waveforms - Continued (sheet 22)

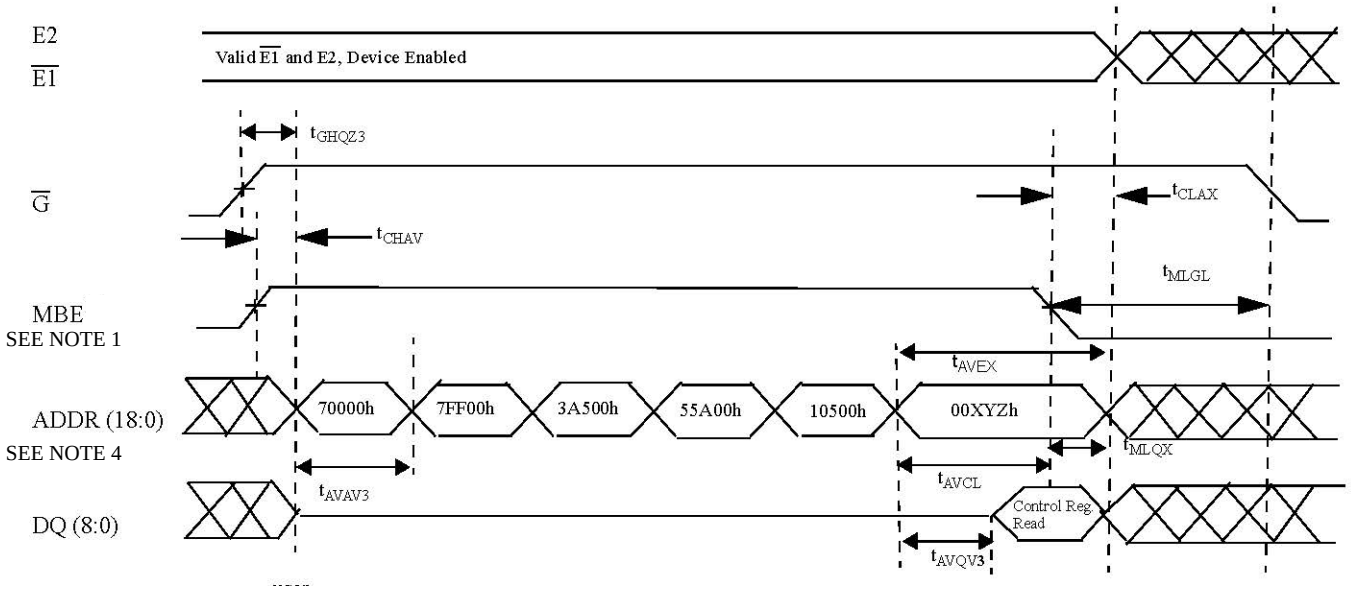
Previous:



Notes:
1. MBE is driven high by the user.
2. Lower 9 bits of the last address are used to read or configure the control register (see vendor data sheet)
3. $\overline{SCRUB} \geq V_{OH}$ before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

EDAC Control register cycle

Corrected:



Notes:
1. MBE is driven high by the user.
2. Lower 10 bits of the last address are used to read or configure the control register (see vendor data sheet)
3. $\overline{SCRUB}$ ≥ V_{OH} before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.
4. Device must see a transition to address 70000h coincident with or subsequent to MBE assertion.

EDAC Control register cycle