APPLICATION NOTE

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AN-LVDS-009-01

Internal and External Failsafe Biasing for the LVDS Receivers

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC
3.3-Volt Quad Receiver	UT54LVDS032LV/E	5962-98652	02, 03, 04, 05	WD04, WD08, WD29, WD31
3.3-Volt Quad Receiver with Termination Resistor	UT54LVDS032LVT	5962-04201	01, 02	WD06, WD10
3.3V Dual Driver and Receiver	UT54LVDM055LV	5962-06202	01	WD22
5.0V Quad Receiver	UT54LVDS032	5962-95834	02	JR06, JR09
5.0V Quad Receiver with Cold Spare	UT54LVDSC032	5962-95834	03	JR11
3.3V Quad Bus LVDS Crosspoint Switch	UT54LVDM228	5962-01537	01	WD15, WD16
3.3V Octal Bus LVDS Repeater	UT54LVDM328	5962-01536	01	WD17, WD18
3.3V LVDS Deserializer	UT54LVDS218	5962-01535	01, 02	WD12, WD14

1.0 Overview

The CAES Colorado Springs LVDS Receiver devices contain internal failsafe circuitry designed to source/sink a small amount of current providing a stable HIGH output state. Supported failsafe configurations are open, shorted, and terminated (100Ω). External failsafe biasing may be added to increase noise tolerance and improve the reliability of internal failsafe circuitry. External failsafe circuitry is not required for all designs; every application should be evaluated to determine if external failsafe circuitry is required. The following Application Note provides a summary of the internal failsafe circuitry and example calculation for selecting external failsafe circuitry. Each of the devices listed in Table 1 have the same failsafe circuitry.

2.0 Failsafe Configurations

The LVDS receiver family are high gain, high speed devices that amplify a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receivers, an evaluation of the system noise should be completed to ensure that noise will not appear as a valid signal. The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated, or shorted receiver inputs.

An open input, as shown in Figure 1, is described as an unused LVDS channel(s) that are left floating. Contrary to good design practice, the unused LVDS inputs on the receivers listed in Table 1 may be left unterminated and floating, i.e. it is not necessary to tie unused receiver inputs to ground or other voltages. The internal failsafe circuitry set the output to a HIGH state. This internal circuitry guarantees a HIGH, stable output state for open inputs in low noise systems (less than ~20mV noise)

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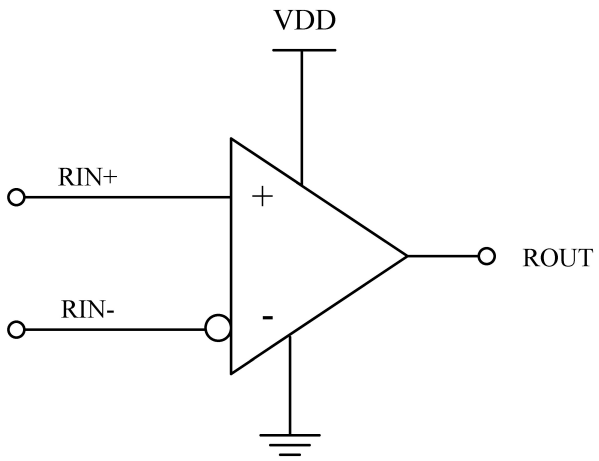

Figure 1. Open Failsafe configuration

Terminated input conditions, as shown in Figure 2, exist if the LVDS driver is disconnected (cable unplugged), or if the driver is in a three-state or power off condition, the receiver output, will again, be in a HIGH state. If there is a cable connected to the receiver end of the LVDS channel and it is unplugged at the driver end, the unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To ensure that any noise is seen as common-mode and not differential, a balanced interconnect should be used and the system designer should consider using external failsafe resistors.

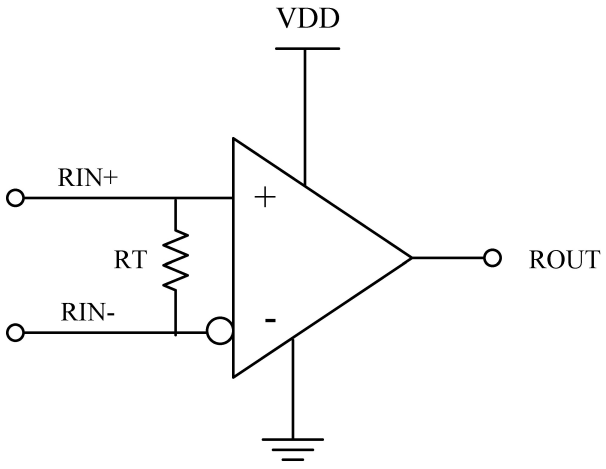

Figure 2. Terminated Failsafe Configuration

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Shorted inputs can occur if a fault condition leaves the receivers LVDS inputs shorted together, thus resulting in a 0V differential input voltage as shown in Figure 3. The receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (VSS to 2.4V). It is only supported with inputs shorted together and no external common-mode voltage applied.

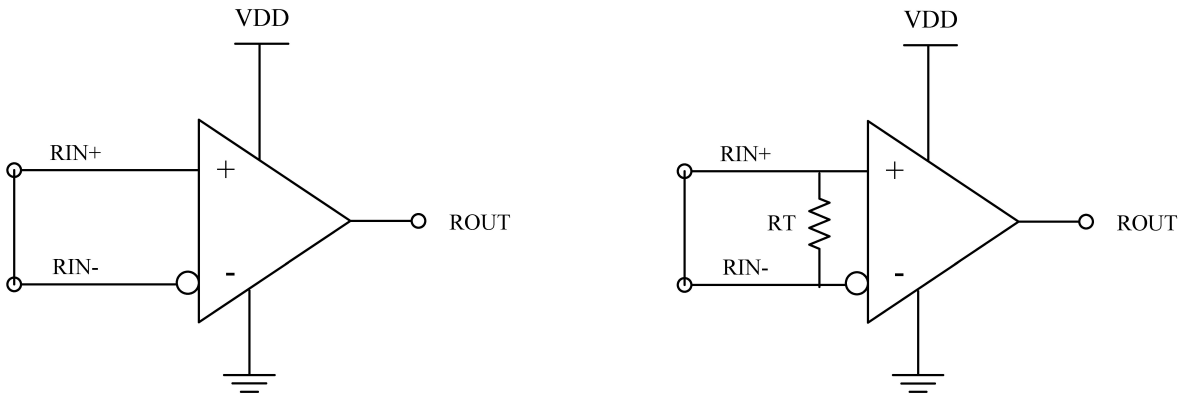

Figure 3. Shorted Failsafe Configurations

3.0 Failsafe Operation

The CAES Colorado Springs LVDS Receiver family implements the internal failsafe function by using small current sources integrated into the receiver. Pull-up and pull-down current sources each capable of sourcing/sinking ~6.5μA ensure that a DC voltage is maintained across the termination resistor when valid input signals are not present, see Figure 4. There is also a small offset built into the internal comparator of the receivers which support the shorted and open failsafe configurations.

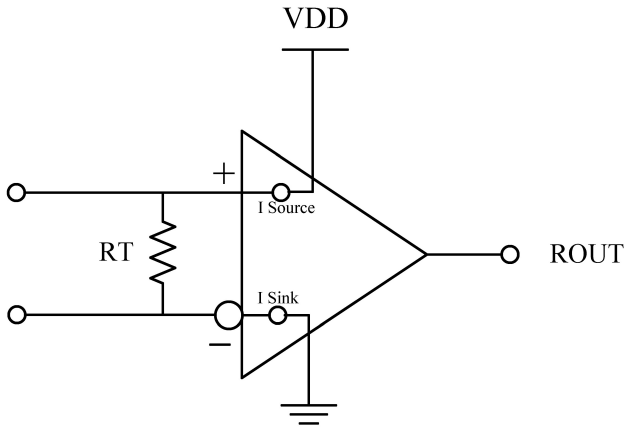

Figure 4. Notional Diagram of Internal Failsafe Circuitry

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These bias sources provide a current which flows through the termination resistor (R_T) insuring that a DC voltage is maintained across the termination resistor when a no valid input is present. The internal logic detects this current across the resistor and drives the output to a known state (HIGH).

4.0 Selecting External Resistor Values

Additional failsafe circuitry may be required if the system is noisy. External resistor values should be selected based on the specific application.

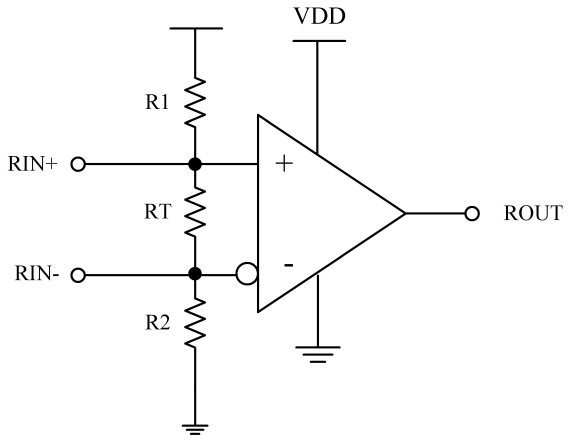

Figure 5. External Failsafe Biasing

R1 and R2, as shown in Figure 5, should be selected such that there is minimal impact on the signal integrity of the LVDS signal. If the bus is shorted or terminated with no driver, the common mode voltage (V_{CM}) needs to be near 1.2V for optimal operation of the receiver sense-amps. Additional failsafe current tends to unbalance the symmetry of the signal. At low data rates external failsafe circuitry may not affect the signal when the receiver is being operated normally, but higher data rates (operation at >100MHz) could be affected by the additional circuitry. All this must be taken into account when selecting the external failsafe resistors.

5.0 Example Calculation

Using a standard 3.5mA UT54LVDS031LV Driver connected to a UT54LVDS032LV Receiver as shown in figure 6, calculate the required values of R1 and R2.

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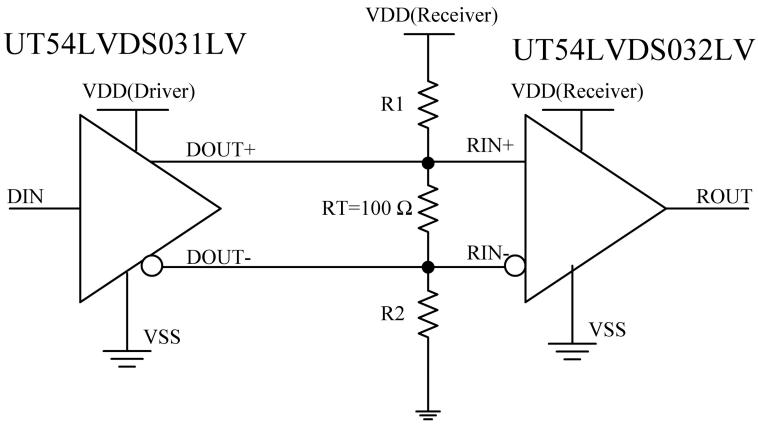

Figure 6. Example Configuration

Note: some receivers may be driven my 10mA LVDM devices, adjust this example accordingly
The bias current should be a least an order of magnitude smaller than the 3.5 mA LVDS Driver current

Definition of Terms:	
V_{CM}	Common Mode Voltage
V_{DD}	Supply Voltage
V_{ISFB}	Internal Failsafe Bias Voltage
R_T	Termination Resistor
R_1	Positive Differential Failsafe Resistor to Supply Voltage
R_2	Negative Differential Failsafe Resistor to Ground
R_{BSTG}	Total Resistance from the Bias Supply to Ground
I_{ISFB}	Internal Failsafe Bias Current

$V_{CM} =\sim 1.25V$
$V_{IFSB} =\sim 20mV$
$R_T = 100\Omega$

Using Ohm's Law calculate the Internal Failsafe Bias Current, I_{ISFB}, using the known Internal Failsafe Bias Voltage, V_{ISFB}.

Ohm's Low: $V = \frac{I}{R}$ or $I = \frac{V}{R}$

For our application use: $I_{IFSB} = \frac{V_{ISFB}}{R_T} = \frac{20mV}{100\Omega} = 200\mu A$

Using Ohm's Law again, calculate Total Resistance from the Bias Supply to Ground, R_{BSTG}.

$R_{BSTG} = \frac{V_{DD}}{I_{ISFB}} = \frac{3.3V}{200\mu A} = 16.5k\Omega$

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The ratio of R_2 to R_1 is calculated using equation 2

$$R_1 / R_2 \approx \frac{V_{CM}}{V_{DD}} \approx \frac{R_1}{R_1 + R_2 + R_T} \approx \frac{R_2}{R_{BSTG}}$$

$$R_1 / R_2 = \frac{V_{CM}}{V_{DD}} = \frac{1.25V}{3.3V} = 0.378$$

** R_T is small (100Ω vs.16.5kΩ) and it can be ignored **

$$R_2 = (R_1 / R_2)(R_{BSTG}) = (0.378)(16.5k\Omega) = 6.23k\Omega$$

$$R_1 = R_{BSTG} - R_2 = 16.5k\Omega - 6.23k\Omega = 10.26k\Omega$$

This network will provide a bias of +20mV to the receiver (V_{IFSB})

6.0 Conclusion

The CAES Colorado Springs LVDS Receiver devices contain internal failsafe circuitry that ensure the output of the device is in a known HIGH state. Supported Failsafe configurations are open, shorted, and terminated (100 Ω).

Depending on the system noise external failsafe biasing resistors may be added to increase noise tolerance and improve the reliability of internal failsafe circuitry.

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