

Application Note



Using the External Data Interface on the 2050 Series Digital & Vector Signal Generators



The external data interface on 2050 series signal generators allows greater flexibility of digital modulation capabilities

Introduction

Digital techniques for communication systems have expanded rapidly over the last decade. The advantages over the traditional analogue systems are the improved spectral efficiency, excellent security and relative immuni-

ty to interference.

As more digital systems are developed engineers need to test and simulate them under a variety of different circumstances. The 2050 series of digital and vector signal generators are ideally suited to this environment and can

be used to simulate present and future modulation formats.

Digital Data Constellation Maps

Below are shown some of the modulation types supported by the 2050 series. The different formats use from 1 to 8 data bits per symbol. To supplement the internal data generator (PRBS, all 0's, all 1's) the auxiliary connector allows the use of an external data generator with the data organized in parallel or serial format. The data is mapped onto the constellation diagram in a format fixed by the internal digital hardware. If other different data to the constellation mappings given are required, these can be implemented by the use of simple external circuits as described later in this application note.

BPSK

The binary phase shift keying, (BPSK or 2PSK) constellation is shown in fig. 1. This requires a single data bit with data of '0' corresponding to point P0 and data of '1' corresponding to point P1.

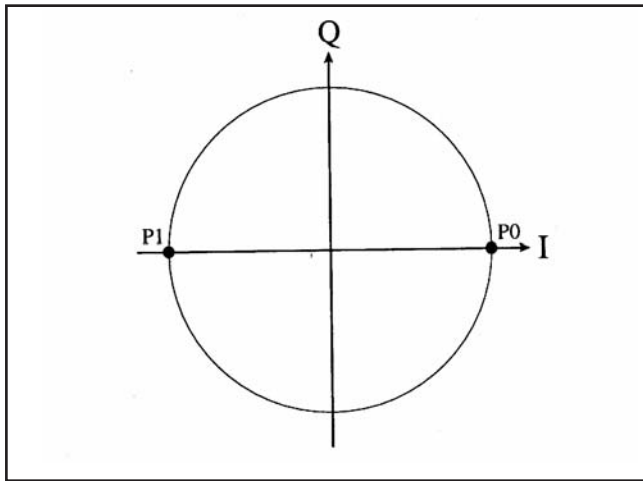


Figure 1. - The BPSK constellation

8PSK

The constellation shown in fig. 2 is for 8PSK. This requires 3 data bits to give 1 of 8 possible constellation points shown as points P0 to P7. The mapping function used by 2050 is shown as follows:

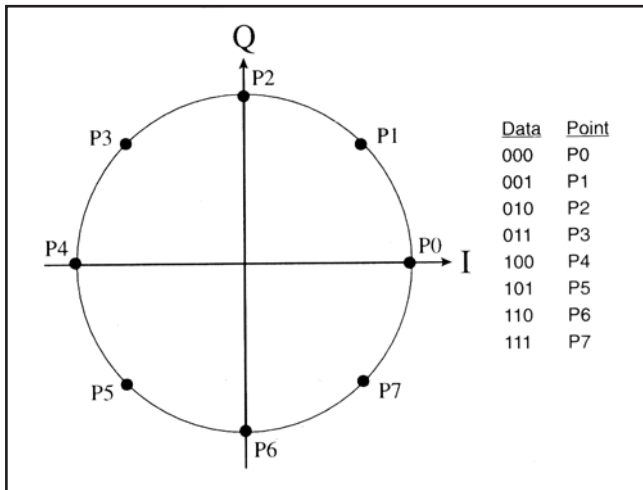


Figure 2 - The 8PSK constellation

$\pi/4$ Differential QPSK

The $\pi/4$ DQPSK format shown in Fig. 3, is used in systems such as the North American Digital Cellular system (NADC) and Japan's Pacific Digital Cellular system (PDC). It uses 2 bits of data to represent each symbol and the phase change between points is defined by this data, rather than each point being allocated to a unique set of data as in normal PSK. This has the advantage of the vector not passing through the origin as it travels between decision points and hence the modulated signal never has an amplitude of zero. The phase change may be defined as follows:

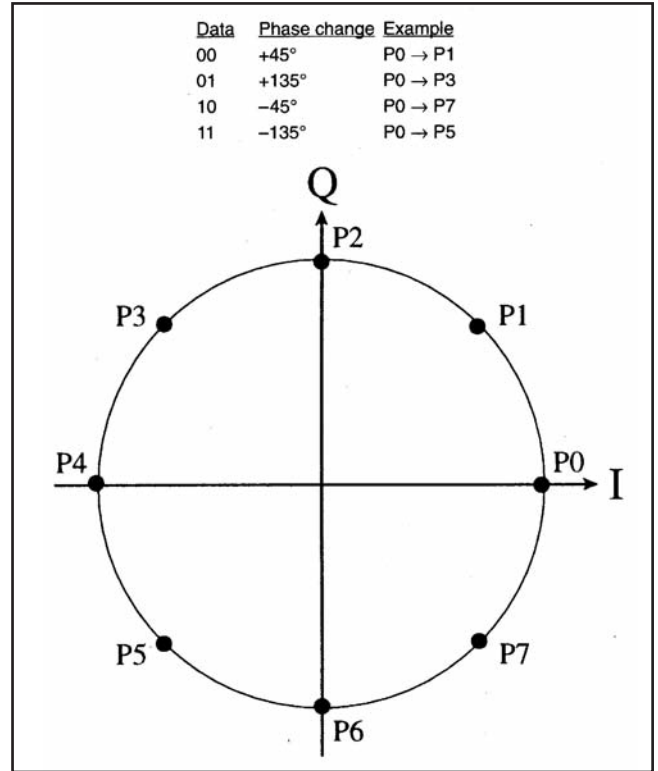


Figure 3 - $\pi/4$ DQPSK constellation

QAM

Quadrature amplitude modulation (QAM) is supported at 4 levels with the 2050 series: 4QAM, 16QAM, 64QAM and 256QAM which need 2, 4, 6 and 8 data bits per symbol respectively. An example of 16QAM is shown in fig. 4. All QAM modulation types are defined in the 2050 series with top left corner being state 0 and bottom right corner for the highest state.

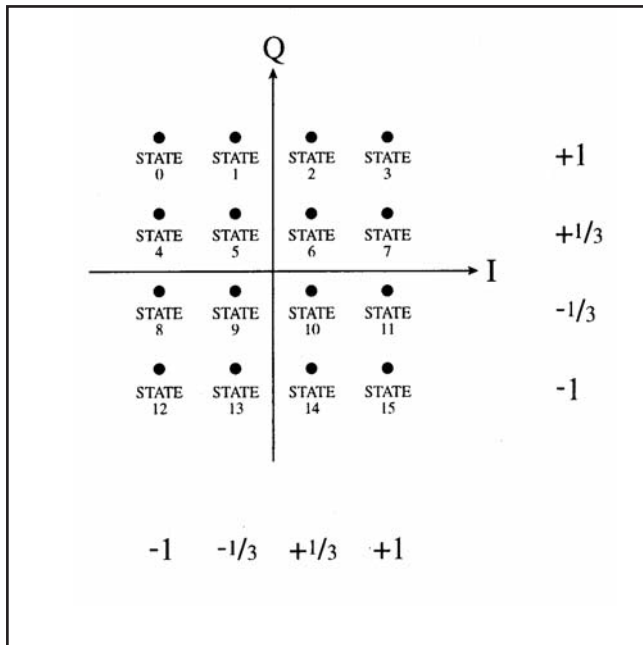


Figure 4 - An example of 16QAM

The Auxiliary Connector

The digital data source of external data can be applied to the 25-way D-type connector on the rear panel. The pin designations for the connector, together with brief descriptions of their functions are shown in Fig. 5.

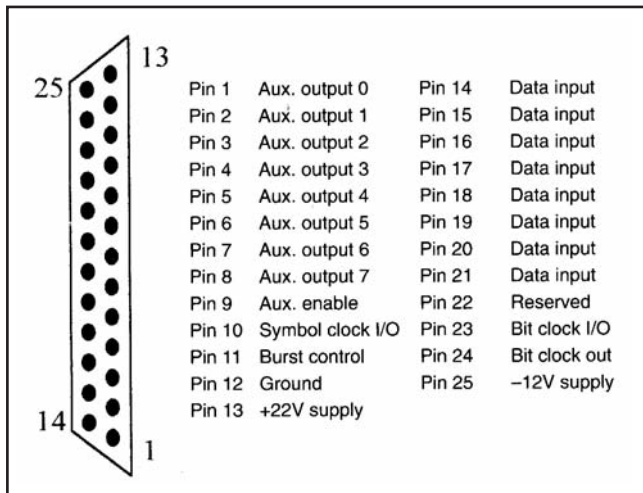


Figure 5 - The auxiliary data connector and pin designations

Auxiliary Outputs

The auxiliary outputs are logic level outputs on pins 1-8 that can be controlled via the "latch poking" utility in Utilities Menu 2 of the 2050. The outputs are enabled by connecting pin 9 to +5 Volts (or logic 1) and are tri-state if pin 9 is connected to 0 Volts (or logic 0) and can be used to control or select external devices.

Data Clocks

There are two data clocks that may be used with external digital data. These are the bit clock and symbol clock. If the signal generator is set to accept parallel data inputs only a symbol clock is required. If the signal generator is set to accept serial data then both symbol and bit clocks are required. The clock signals are connected to pins 10 & 23 respectively and are bi-directional. This allows the flexibility to apply either externally generated clocks and data together, or to use clocks generated internally by the 2050 to synchronize your own external data into the digital modulator. The latter method eliminates timing jitter from external data sources.

The timing requirements for these are given in more detail in the next section.

All clocks and data lines are TTL/CMOS compatible.

Power Supply Outputs

There are two power supply outputs available to the user which may be used to power external equipment, such as a data generator. These supplies are +22 V and - 12 V and are available on pins 13 and 25 respectively. Each can provide 300 mA. The ground return is on pin 12 for both the power supplies and the digital data.

By using suitable voltage converters or voltage regulators, common voltages such as +12 V, +5 V and - 5 V can be generated. As an example, +5 V can be generated using a standard 78L05 to power +5 V logic circuits.

Digital Data Inputs

There are eight data inputs on pins 14-21. Their designations are shown in the table below for various data formats. The data format used is either serial or 2 to 8 bit parallel data and any of these can be selected via the front panel setup of the 2050.

Serial data is applied to pin 21. For parallel data, the data is allocated from pin 21 to pin 14 with pin 21 being the most significant data bit. In the case of 8-bit parallel data, D7 (most significant data bit) is assigned to pin 21 and D0 (least significant data bit) is assigned to pin 14 as shown in Fig. 6.

| Data format | Pin 14 | Pin 15 | Pin 16 | Pin 17 | Pin 18 | Pin 19 | Pin 20 | Pin 21 |
|----------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Serial | X | X | X | X | X | X | X | Data |
| 2-bit parallel | X | X | X | X | X | X | D0 | D1 |
| 3-bit parallel | X | X | X | X | X | D0 | D1 | D2 |
| 4-bit parallel | X | X | X | X | D0 | D1 | D2 | D3 |
| 5-bit parallel | X | X | X | D0 | D1 | D2 | D3 | D4 |
| 6-bit parallel | X | X | D0 | D1 | D2 | D3 | D4 | D5 |
| 7-bit parallel | X | D0 | D1 | D2 | D3 | D4 | D5 | D6 |
| 8-bit parallel | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |

Figure 6 - Data inputs for serial and parallel data

Burst Control Input

The burst control input, assigned to pin 11, is used to turn the RF signal on or off with a controlled rise/fall time. When the input is uncommitted or connected to +5 V the 2050 will give the requested power level. Applying 0 V (or logic 0) will result in the signal being switched off. The rise and fall time of RF power is internally controlled to occur over 3 symbol clocks to simulate an RF burst of modulated carrier as used in TDMA or TDD systems as shown in fig. 7.

There is a delay between the switching of the burst control and the change of RF power is synchronized to match the data delay.

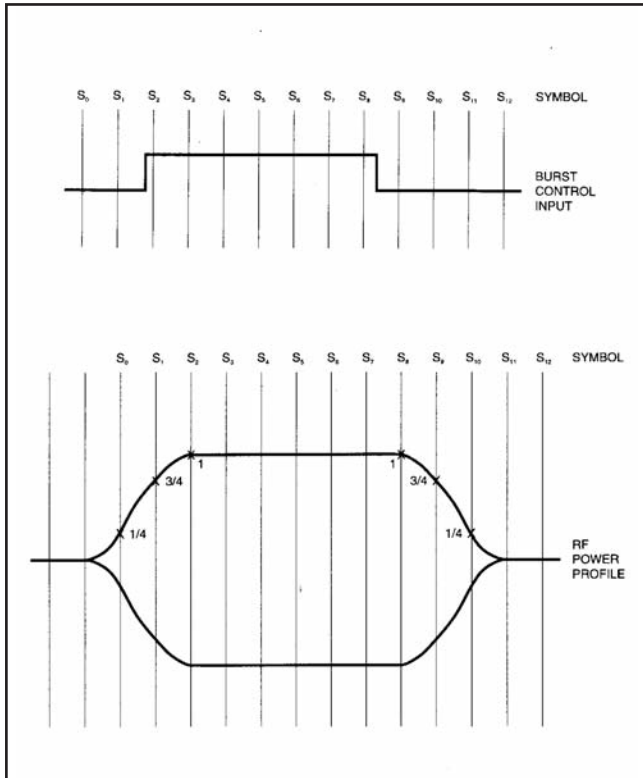


Figure 7 - Effect of the burst control on RF output level

Setting Up The External Inputs

With the 2050 configuration shown in fig. 8 the external data changes on the rising edge of the bit clock and symbol clock. It should be noted that both the bit clock and the symbol clock can be defined as negative or positive edge triggered.

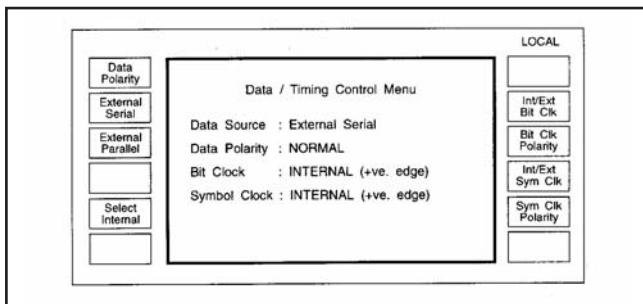


Figure 8 - A typical 2050 external data configuration screen

For the case where the user selects positive edge triggered clocks, the data should change on these positive edges as shown

in Fig. 9. For negative edge triggered clocks, the data should change on the negative edge. For serial data, it can be valid to have a positive edge triggered symbol clock and a negative edged triggered bit clock, or vice versa. For parallel data, the hardware must accept the valid data from the external interface by loading it into the digital modulation processor. It is clocked using the timing diagram shown in Fig. 9.

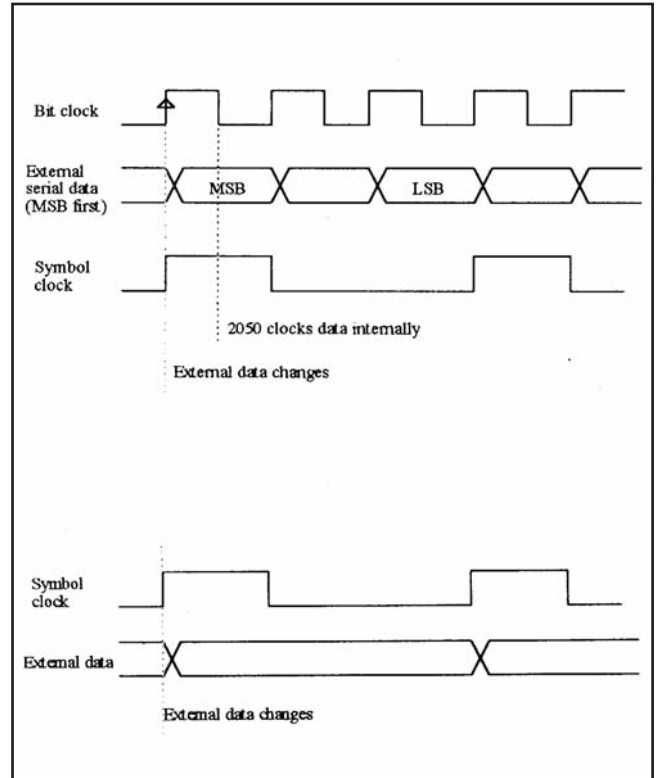


Figure - 9 External timing for 3-bit serial data and n-bit parallel data formats

The Break-Out Box

A "break-out" box (IFR part no. 44991/144) is available as an optional accessory. This can be connected to the auxiliary data connector on the 2050 and allows the data lines and clocks to be accessed via BNC connectors as shown in Fig. 10.

A through connection is available to allow the 25-way D-type to be used with the signals being monitored via the "break-out" box.

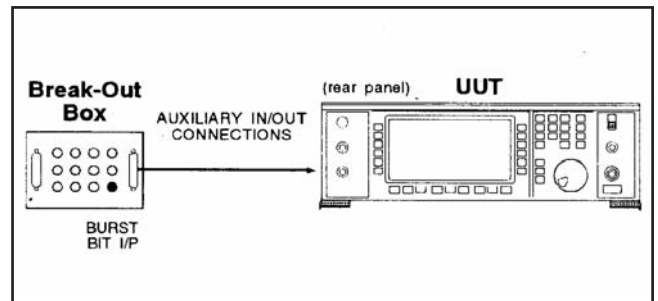


Figure 10 - The "Break-out" Box connected to the 2050

Using the External Data Interface ROM Based External Data Generator

It is possible to program an external memory device with

sequences of data symbols and then clock these into the 2050 data inputs using the symbol clock as shown in fig. 11. If a positive triggered symbol clock is defined for the 2050 then this can clock a memory address counter. The data from the memory device is then presented to the 2050 data inputs and clocked into the unit on the negative edge of the clock. One of the auxiliary output lines can be used as a reset and another as an inhibit if required. In the example shown, the 8k byte EPROM is divided into 4 sets of 2k symbols, the set being used is defined by two of the auxiliary outputs. The symbols may be 1-8 bits and the redundant EPROM outputs are ignored by the 2050. The complete external circuit is powered from the supplies available on the auxiliary connector, regulated to the required voltage.

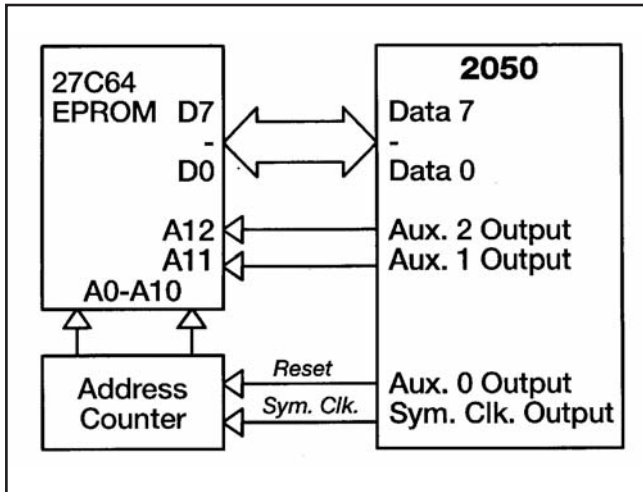


Figure 11 - An example of a ROM based data generator

This idea can be expanded to use larger memories with differently partitioned areas. If 7 or less bits per symbol are used (all systems except 256QAM) one of the data lines from the memory could be used as a burst control bit to allow power profiling of the RF output.

Re-defining the Data Inputs to Suit the User's Application

There are many ways that the applied digital data can be mapped to a non-standard format with the 2050. Possible solutions are shown here for two different problems, both involving a look-up table constructed using an EPROM. This can be the case if the mapping used by the user is different to those designated by the 2050. Fig. 12 shows the 8PSK mapping defined by the 2050 and the user's mapping requirement.

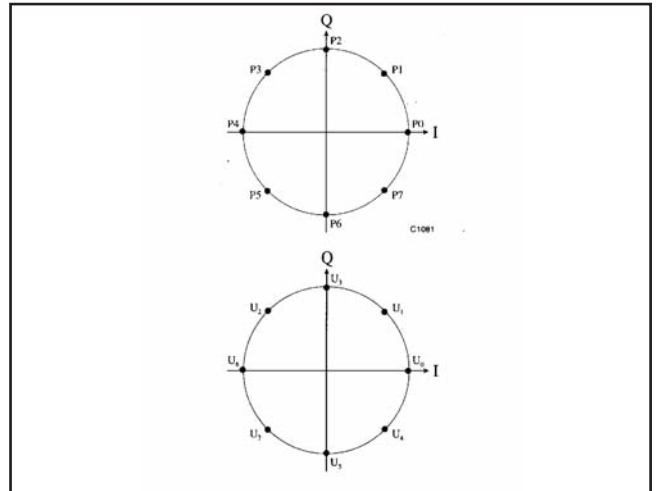


Figure 12 - 8PSK defined by the 2050 and the user

To re-map this data requires an 8x3 bit EPROM. The user's 3 bits of data become the address for the EPROM and the 3 bit output of this device is connected to the lower 3 bits of the 2050 external data interface. The EPROM is set up as shown below.

A larger, standard EPROM may be used with the upper address lines tied to ground and all addresses above 00H-07H left empty. Only the 3 lower data bits would be used to interface to the 2050.

| User's point | Data (EPROM address) | 2050 point | Data (EPROM output) | EPROM data HEX |
|--------------|----------------------|------------|---------------------|----------------|
| U0 | 000 | P0 | 000 | 00H |
| U1 | 001 | P1 | 001 | 01H |
| U2 | 010 | P3 | 011 | 03H |
| U3 | 011 | P2 | 010 | 02H |
| U4 | 100 | P7 | 111 | 07H |
| U5 | 101 | P6 | 110 | 06H |
| U6 | 110 | P4 | 100 | 04H |
| U7 | 111 | P5 | 101 | 05H |

Simulating a 32QAM System Using the 64QAM Modulation

A similar example is 32QAM which can be generated using the 64QAM format, re-mapping the data and omitting the outer states. The mapping is shown in Fig. 13. Assuming for 64QAM that P0 is the top left point of the constellation, followed by other points going left to right and then onto the next row. The 32QAM is defined with U0 as position P10 on the 64QAM mapping. The user's 5-bit data for 32QAM defines the lower five bits of the EPROM address and the EPROM outputs are then re-mapped points for the 64QAM system. The re-mapping is done in a similar way to that of the previous example:

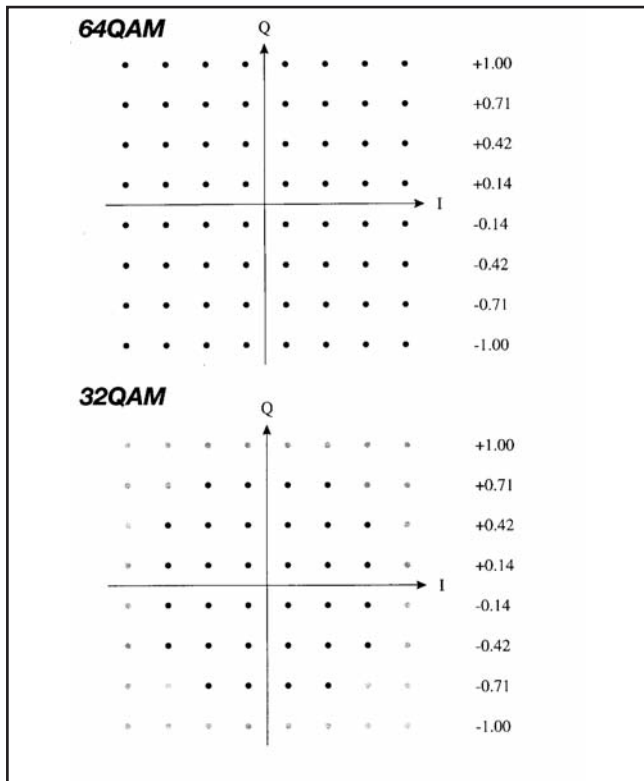


Figure 13 - Remapping 64QAM to provide 32QAM

If a 2716 EPROM is used then the address lines A9 to A0 are available. Address lines A9 to A5 are connected to 0 V and address lines A4 to A0 are used for the user's 32QAM data. The EPROM outputs are Q7 to Q0 where Q5 to Q0 are connected to the 2050 auxiliary connector. Although the EPROM contains 2048 8-bit words, the user only needs to program the first 32 bytes with the data below.

| User's point | Data (EPROM address) | 2050 point | Data (EPROM output) | EPROM data HEX |
|--------------|----------------------|------------|---------------------|----------------|
| U0 | 00000 | P10 | 001010 | 0AH |
| U1 | 00001 | P11 | 001011 | 0BH |
| U2 | 00010 | P12 | 001100 | 0CH |
| U3 | 00011 | P13 | 001101 | 0DH |
| U4 | 00100 | P17 | 010001 | 11H |
| ↓ | ↓ | ↓ | ↓ | ↓ |
| U30 | 11110 | P52 | 110100 | 34H |
| U31 | 11111 | P53 | 110101 | 35H |

The user needs to apply a power level correction to the modulated carrier as the data no longer uses the full range of the I-Q modulator.

Auxiliary Latch Outputs and Power Supplies

An application for these latched outputs is band switching between external band-pass filters to remove the unwanted mixing products inherent in the 2050 architecture or to switch between external amplifiers for high power transmitter simulation. The +22 V and - 12 V power supplies which are available can be used to drive co-axial switches in these applications. It should be noted that these outputs and supplies can be used independently of the digital and vector facilities of 2050. The user can connect an external system to the auxiliary connector and control it via the

GPIB by addressing the latch for the auxiliary outputs as shown on the 2050 utility screen in Fig. 14.

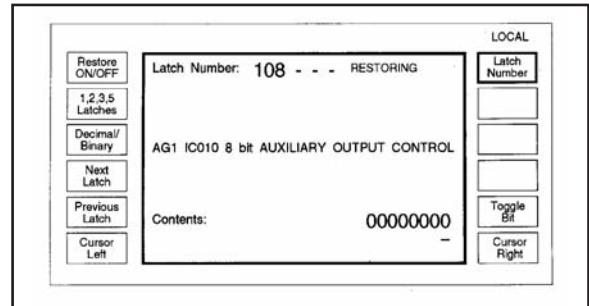


Figure 14 - Latch poking the auxiliary outputs

Bit Error Rate Testing

The 2050 signal generator can be used for bit error testing to assess the receiver performance under a number of conditions.

Digital data is applied to the 2050 data interface and used to provide a digitally modulated signal. This can be decoded by the receiver and a bit error rate test performed by comparing the demodulated data to that applied to the 2050 as shown in Fig. 15. If PRBS data is generated from a 2851 then the receiver will automatically time align. The user can then use the functions of generating modulation errors within the 2050, such as I-Q gain imbalance, carrier leak and I-Q skew or to use the fading simulation to check the performance of the receiver under test to adverse conditions by comparing the relative bit error rates. Modulator errors can be introduced by using the 'IQ error' menu facility in 2050 as shown in Fig. 15.

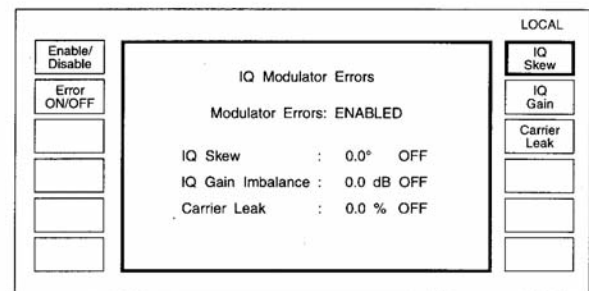
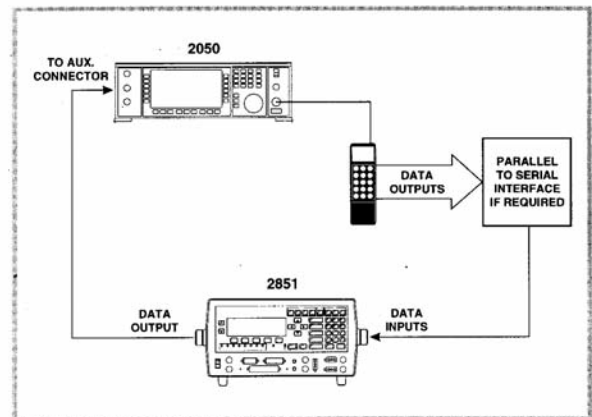


Figure 15 - A typical set-up for bit error rate testing with IQ modulator errors

Complementary Publications

IFR has published other application notes relevant to the digital modulation capabilities of 2050 series. Some of these are listed below:

- An Introduction to Digital & Vector Modulation (Publication no. 46891-863)
- Fading & Multipath (Publication no. 46889-472)
- Generating Radar Chirp Signals (Publication no. 46889-472)
- Signal Generator for Generating DECT Signals (Publication no. 46889-450)
- An Introduction to D-Amps (Publication no. 46889-458)

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